APPLICATION

FOR

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TITLE: PHASE CHANGE MATERIAL MEMORY DEVICE

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PHASE CHANGE MATERIAL MEMORY DEVICE

Background

This invention relates generally to electronic memories and particularly to electronic memories that use phase change material.

Phase change materials may exhibit at least two different states. The states may be called the amorphous and crystalline states. Transitions between these states may be selectively initiated. The states may be distinguished because the amorphous state generally exhibits higher resistivity than the crystalline state. The amorphous state involves a more disordered atomic structure. Generally any phase change material may be utilized. In some embodiments, however, thin-film chalcogenide alloy materials may be particularly suitable.

The phase change may be induced reversibly. Therefore, the memory may change from the amorphous to the crystalline state and may revert back to the amorphous state thereafter, or vice versa, in response to temperature changes. In effect, each memory cell may be thought of as a programmable resistor, which reversibly changes between higher and lower resistance states. The phase change may be induced by resistive heating.

In some embodiments, the cell may have a large number of states. That is, because each state may be distinguished by its resistance, a number of resistance determined states may be possible, allowing the storage of multiple bits of data in a single cell.

A variety of phase change alloys are known. Generally, chalcogenide alloys contain one or more elements from Column VI of the periodic table. One particularly suitable group of alloys is the GeSbTe alloys.

A phase change material may be formed within a passage or pore through an insulator. The phase change material may be coupled to upper and lower electrodes on either end of the pore.

One problem that arises with existing lower electrodes is that some suitable lower electrode materials that have advantageous properties cannot be used because they may be adversely affected by necessary subsequent processing steps or upon exposure to the open environment. Among the advantageous attributes of the lower electrode material is good electrical contact to phase change materials and effective resistive heating to promote more efficient phase change programming.

Thus, there is a need for better designs for phase change memories that may be manufactured using more advantageous techniques.

Brief Description of the Drawings

Figure 1 is an enlarged, cross-sectional view in accordance with one embodiment of the present invention;

Figure 2 is an enlarged, cross-sectional view of the device shown in Figure 1 taken transversely to the view shown in Figure 1;

Figure 3 is a top plan view of the embodiment shown in Figures 1 and 2;

Figure 4 is an enlarged cross-sectional view of the initial processing of the structure of Figure 1 in accordance with one embodiment of the present invention;

Figure 5 shows subsequent processing on the structure shown in Figure 4 in accordance with one embodiment of the present invention;

Figure 6 shows subsequent processing of the structure shown in Figure 5 in accordance with one embodiment of the present invention;

Figure 7 shows subsequent processing of the embodiment shown in Figure 6 in accordance with one embodiment of the present invention;

Figure 8 shows subsequent processing of the embodiment shown in Figure 7 in accordance with one embodiment of the present invention; and

Figure 9 shows subsequent processing of the embodiment shown in Figure 8 in accordance with one embodiment of the present invention.

Detailed Description

Referring to Figure 1, a phase change memory cell 10 may be formed on a substrate 12 that in one embodiment may be a silicon substrate. A pair of lower electrodes 14 may be formed over the substrate 12. The electrodes 14 may be separated by an insulator 16. Furthermore, the electrodes 14 may be covered by a protective film 40. In some embodiments, an optional base material 42 may be formed over the substrate so that the electrode 14 is sandwiched between the base material 42 on the bottom and the protective film 40 on the top.

A pore may be formed above the lower electrode 14 between the lower electrode 14 and the top electrode 28. The pore may include a tapered, cup-shaped phase change material 18 covered by a similarly shaped barrier layer 20. A fill insulator 22 may fill the central portion of the barrier 20 and the phase change material 18. An etch stop layer 24 underlies a barrier layer 26 that in turn underlies the top electrode 28.

Referring to Figure 1, the top electrode 28 extends along at least two adjacent pores. The pores may be separated by an insulator 16. Cells defined by the pores may be distributed in large numbers across the substrate 12 in some embodiments. As viewed from above in Figure 3, each electrode 28 covers a plurality of pores including the

elements 14, 18, 20 and 22, separated by insulator 16 covered by an etch stop layer 24.

A technique for forming the memory cells 10, according to one embodiment, may involve initially forming the lower electrodes 14 on a substrate 12 using conventional patterning and deposition techniques, as shown in Figure 4.

Referring to Figure 4, a base layer 42 may be deposited on top of the substrate 12 in some embodiments of the present invention. In other embodiments, the base layer 42 may not be utilized. The base layer 42 may be made of material such as cobalt silicide, titanium tungsten or another conductive material.

The lower electrode 14 may be formed over the base layer 42 if utilized. Finally, a protective film 40 may be formed over the electrode 14. The lower electrode 14 may be any of a variety of conductive materials including carbon. The protective film 40 may be chosen from a variety of insulating materials including SiO_2, Si_3N_4 or Al_2O_3. In general, the protective material may also be any material in the form Si_xN_y, where x and y represent the stoichiometry and an advantageous stoichiometry is where x is equal to three and y is equal to four.

The base layer 42, lower electrode 14 and a protective film 40 may be formed sequentially. Advantageously, the lower electrode 14 and the protective film 40 are formed in

situ, for example in the same deposition chamber without venting back to atmosphere.

Referring to Figure 5, the structure shown in Figure 4 may then be subjected to patterning to form the stacks 46a and 46b. Alternatively, each of the three layers 14, 40 and 42 may be separately patterned.

Referring to Figure 6, the insulator 16 may then be deposited over the patterned lower electrode stacks 46. In one embodiment, the insulator 16 is an electrical and thermal insulator. One suitable material is silicon dioxide that may be from about 50 to 1500 Angstroms thick in one embodiment. Next a planarization such as, for example, a chemical mechanical planarization (CMP) is performed to achieve global and local planarity. This may be followed by the deposition, if desired, of a CMP etch stop layer 24. The layer 24 may be silicon nitride or polysilicon having a thickness from 10 to 1000 Angstroms in one embodiment.

Referring next to Figure 7, the pore openings 32, defined through the etch stop layer 24 and protective film 40, receive a side wall spacer 30. The side wall spacer 30 may be formed using standard techniques of depositing an insulating layer and selectively anisotropically dry etching that layer down to the lower electrode 14. The insulating spacer 30 may be made of silicon dioxide or nitride such as Si_3N_4. The thickness of the insulating

spacer 30 may be in the range of 50 to 2000 Angstroms in one embodiment.

Turning next to Figure 8, deposited in a sequential fashion over the structure shown in Figure 7 may be the phase change layer 18, barrier layer 20, and fill insulator 22, in one embodiment. The phase change material 18 may be a chalcogenide-based material such as $Ge_2Sb_2Te_5$ with a thickness of 50 to 1000 Angstroms in one embodiment. The barrier material 20 may be, for example, titanium, titanium nitride or titanium-tungsten, for example, with a thickness in the range of 10 to 500 Angstroms. The fill insulator 22 may be any insulator with low thermal and electrical conductivity. Examples of suitable fill insulator 22 materials include silicon dioxide or silicon nitride, such a Si_3N_4 with a thickness of about 500 to 10,000 Angstroms, for example.

Turning finally to Figure 9, CMP removes the fill insulator 22, barrier layer 20, and phase change material 18 in all regions above the etch stop layer 24. CMP thereby defines the structure of the phase change material 18 while eliminating the need for a dry etch in one embodiment. As mentioned earlier, the use of the dry etch may complicate the process flow and raise issues of undercut and re-entrant profiles. Moreover, because the phase change material 18 is defined within an encapsulated, singulated region, the problem of adhesion between the

phase change material 18 and the surrounding materials may be substantially reduced or even eliminated, even after exposure to ensuing thermal stresses.

The imposition of the insulator 22 over the phase change material 18 reduces upward thermal losses. Thermal losses may result in the need for greater programming currents to obtain the same programming effect.

As shown in Figure 1, the structure of Figure 9 may be covered with a barrier layer 26 and a top electrode 28. In one embodiment, the barrier layer 26 may be titanium, titanium nitride, or titanium-tungsten at a thickness in the range of 10 to 500 Angstroms. The top electrode 28 may be aluminum copper alloy in one embodiment with a thickness in the range of 200 to 20,000 Angstroms. The use of a barrier layer 26 may reduce the incorporation of species from the top electrode 28 into the phase change material 18 in some embodiments. The top electrode 28 and barrier layer 26 may be patterned using standard photolithographic and dry etching techniques to achieve the structures shown in Figure 1, 2, and 3.

In accordance with some embodiments of the present invention, a wider selection of lower electrode 14 material is made available by providing a technique for limiting the exposure of the lower electrode 14 to other process steps or to the open environment. As a result, a purer, less contaminated lower electrode 14 may be achieved in some

embodiments, achieving more consistent, predictable device operation.

While the present invention has been described with respect to a limited number of embodiments, those skilled in the art will appreciate numerous modifications and variations therefrom. It is intended that the appended claims cover all such modifications and variations as fall within the true spirit and scope of this present invention.

What is claimed is: